PRODUCT SPECIFICATION

Z86C08

CMOS Z8® 8-BIT MICROCONTROLLER

FEATURES

- 8-bit CMOS microcontroller
- 18-pin DIP
- Low cost
- 3.0 to 5.5 Volt V_{cc} range
- Low power consumption; 50 mW (typical)
- Brown-Out protection
- Fast instruction pointer; 1 microsecond at 12 MHz
- Two standby modes; STOP and HALT
- 14 Input/Output lines
- All digital inputs at CMOS levels; Schmitt triggered
- 2 KBytes of ROM
- 124 Bytes of RAM.
- Two programmable 8-bit counter/timers each with a 6-bit programmable prescaler.
- Six vectored, priority interrupts from six different sources
- Clock speeds 8 and 12 MHz
- Watchdog/Power-On Reset Timer
- Two Comparators with programmable interrupt polarity.
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, or external clock drive.

GENERAL DESCRIPTION

The Z86C08 Microcontroller Unit (MCU) introduces a new level of sophistication to single-chip architecture. The Z86C08 is a member of the Z8 single-chip microcomputer family with 2 Kbytes of ROM and 124 bytes of general-purpose RAM. The device is housed in an 18-pin DIP, and is manufactured in CMOS technology. The Zilog Z86C08 offers all the outstanding features of the Z8 family architecture, and easy software/hardware system expansion along with low cost, low power consumption.

The Z86C08 is characterized by a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, industrial and advanced scientific applications.

The device applications demand powerful I/O capabilities. The Z86C08 fulfills this with 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals.

There are two basic address spaces available to support this wide range of configurations, Program Memory, and 124 bytes of general-purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and I/O data communications, the Z86C08 offers two on-chip counter/timers with a large number of user selectable modes. Also, there are two on-board comparators that can process analog signals with a common reference voltage (Figure 5).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

GENERAL DESCRIPTION (Continued)

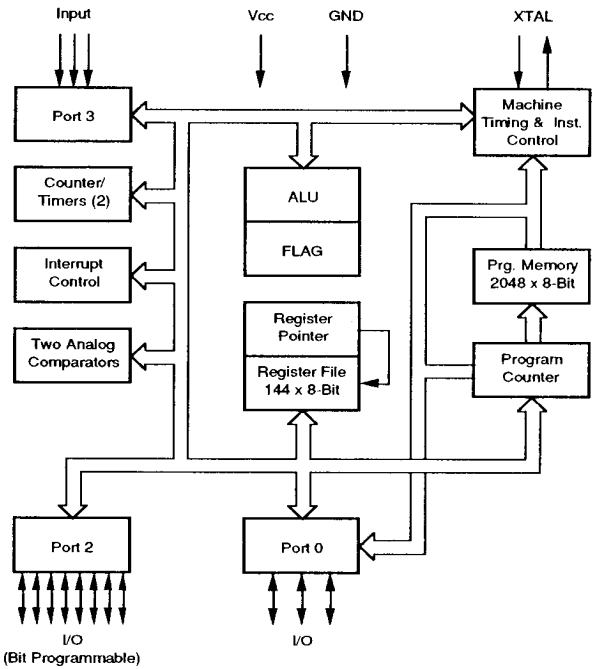


Figure 1. Functional Block Diagram

PIN DESCRIPTIONS AND SIGNAL FUNCTIONS

This Section describes the pin numbers and respective signals plus their functions (Figure 2 and Table 1).

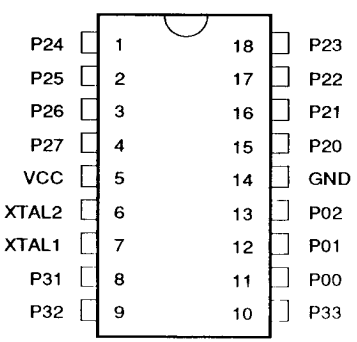


Figure 2. Pin Configuration

Table 1. Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-7	Port 2 pin 4,5,6,7	In/Output
5	V_{cc}	Power Supply, V_{DD}	Input
6	XTAL2	Crystal Oscillator Clock	Input
7	XTAL1	Crystal Oscillator Clock	Output
8	P31	Port 3 pin 1, AN1	Input
9	P32	Port 3 pin 2, AN2	Input
10	P33	Port 3 pin 3, REF	Input
11-13	P00-2	Port 0 pin 0,1,2	In/Output
14	GND	Ground, V_{SS}	Input
15-18	P20-3	Port 2 pin 0,1,2,3	In/Output

XTAL1, XTAL2. *Crystal in, Crystal Out* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (12 MHz max) to the on-chip clock oscillator and buffer.

Port 0 (P00-P02). Port 0 is a 3-bit I/O, nibble programmable, bidirectional, CMOS compatible I/O port. These 3 I/O lines can be configured under software control to be an input or output (Figure 3).

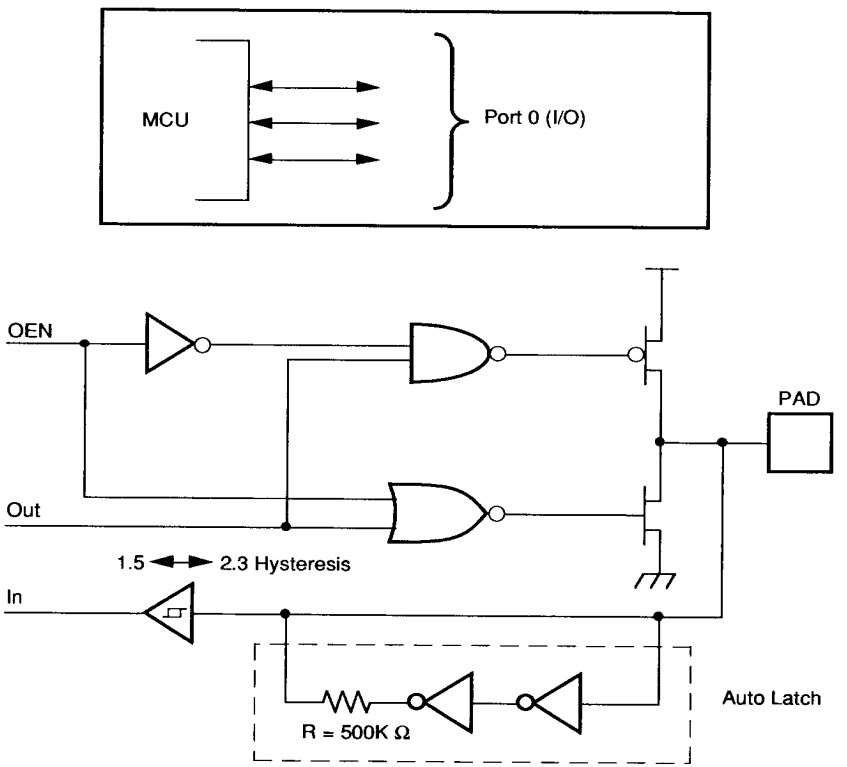


Figure 3. Port 0 Configuration

Port 2 (P20-P27). Port 2 is an 8-bit I/O, bit programmable, bidirectional, CMOS compatible I/O port. These 8 I/O lines can be configured under software control to be an input or output, independently. Bits programmed as outputs may be globally programmed as either push pull or open drain (Figure 4).

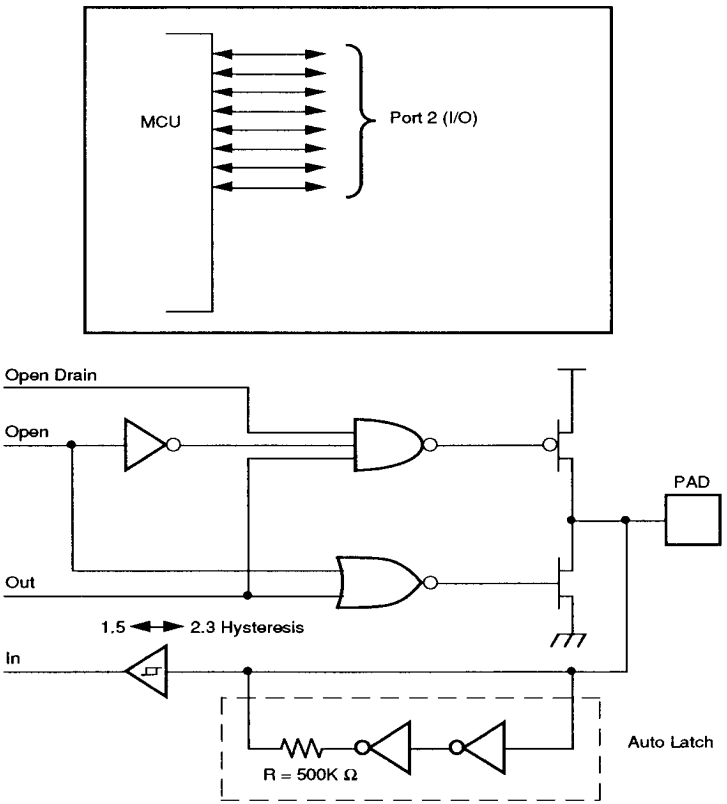
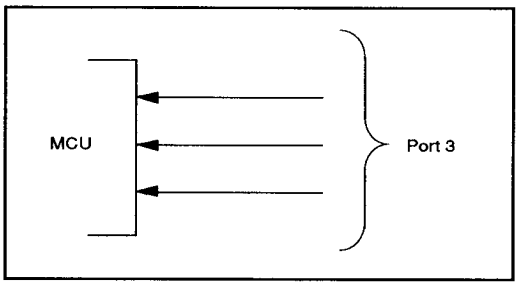


Figure 4. Port 2 Configuration

Port 3 (P31-P33). Port 3 is a 3-bit, CMOS compatible port with three fixed input (P32-P33) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines can also be used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (T_{IN}) (Figure 5).



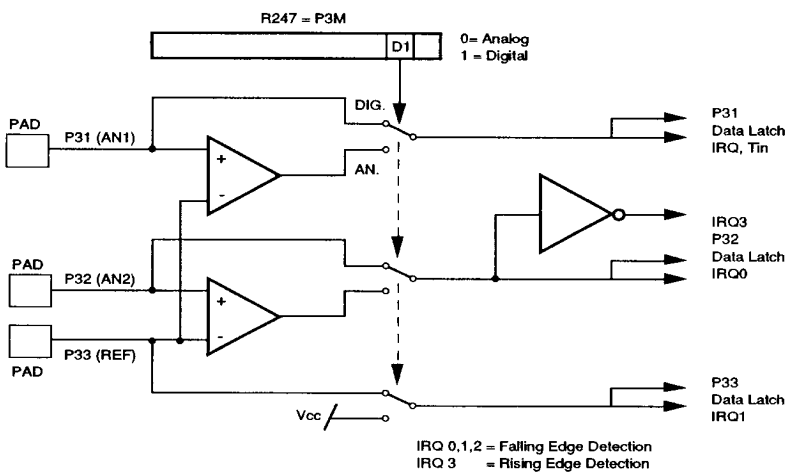


Figure 5. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to Port 3 inputs for interface flexibility.

Typical applications for the on-board comparators are: Zero crossing detection, A/D conversion, voltage scaling, and threshold detection.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4V; the power supply and common mode rejection ratios are 90dB and 60dB, respectively.

Interrupts are generated on either edge of comparator 2's output, or on the falling edge of comparator 1's output. The comparator output may be used for interrupt generation, Port 3 data inputs, or Tin through P31. Alternatively, the comparators may be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The Z8 MCU incorporates special functions to enhance the Z8's application in industrial, scientific research, an advanced technologies applications.

Reset. Upon power up the power-on reset circuit waits for 50 msec plus 18 crystal clocks and then starts program execution at address %000C (HEX) (Figure 6). Reference the Z86C08 control registers' Reset value (Table 2).

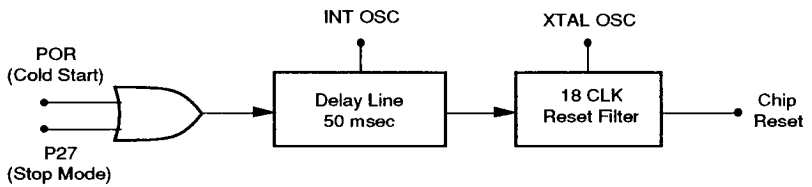


Figure 6. Internal Reset Configuration

Table 2. Z86C08 Control Registers

Addr.	Reg.	Reset Condition D7	D6	D5	D4	D3	D2	D1	D0	Comments
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F7*	P3M	U	U	U	U	U	U	0	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
PB	IMR	0	U	U	U	U	U	U	U	
PC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	0	0	0	0	0	0	0	0	
FE	SPH	U	U	U	U	U	U	U	U	Not used, stack always internal
FF	SPL	U	U	U	U	U	U	U	U	

Note:
* A reset after a low on P27 to get out of stop mode may affect device reliability.

Program Memory. The Z86C08 can address up to 2 Kbytes of internal program memory (Figure 7). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-2048 are on-chip mask-programmed ROM.

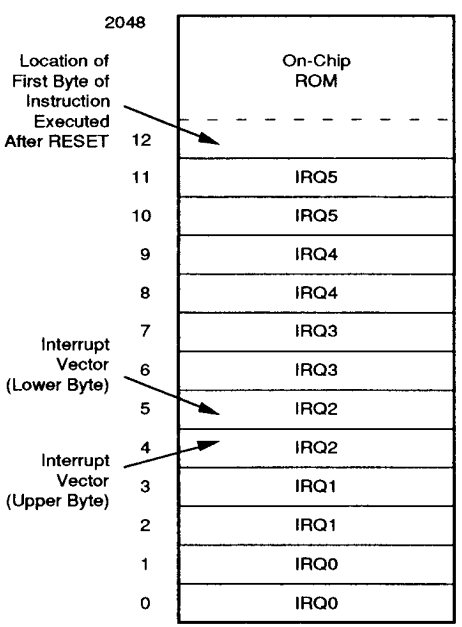


Figure 7. Program Memory Map

Register File. The Register File consists of three I/O port registers, 124 general purpose registers, and 15 control and status registers (R0-R3, R4-R127 and R241-R255, respectively - Figure 8). The Z86C08 instructions can access registers directly or indirectly via an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 9) addresses the starting location of the active working-register group.

Location		Indentifiers
255	Stack Pointer (Bits 7-0)	SPL
254	Reserved	
253	Register Pointer	RP
252	Program Control Flags	Flags
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	To Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240 128	Not Implemented	
127 4	General Purpose Registers	
3	Port 3	P3
2	Port 2	P2
1	Reserved	P1
0	Port 0	P0

Figure 8. Register File

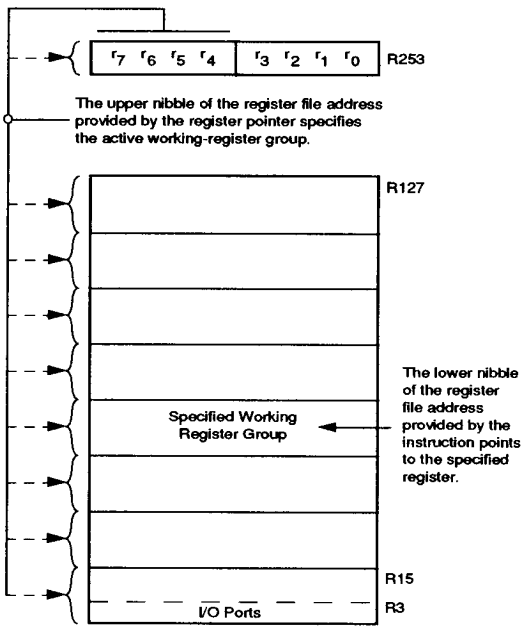


Figure 9. Register File

Stack Pointer. The Z86C08 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 General-Purpose registers.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however the T0 can be driven by the internal clock source only (Figure 10).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that is retriggerable or not retriggerable, or as a gate input for the internal clock.

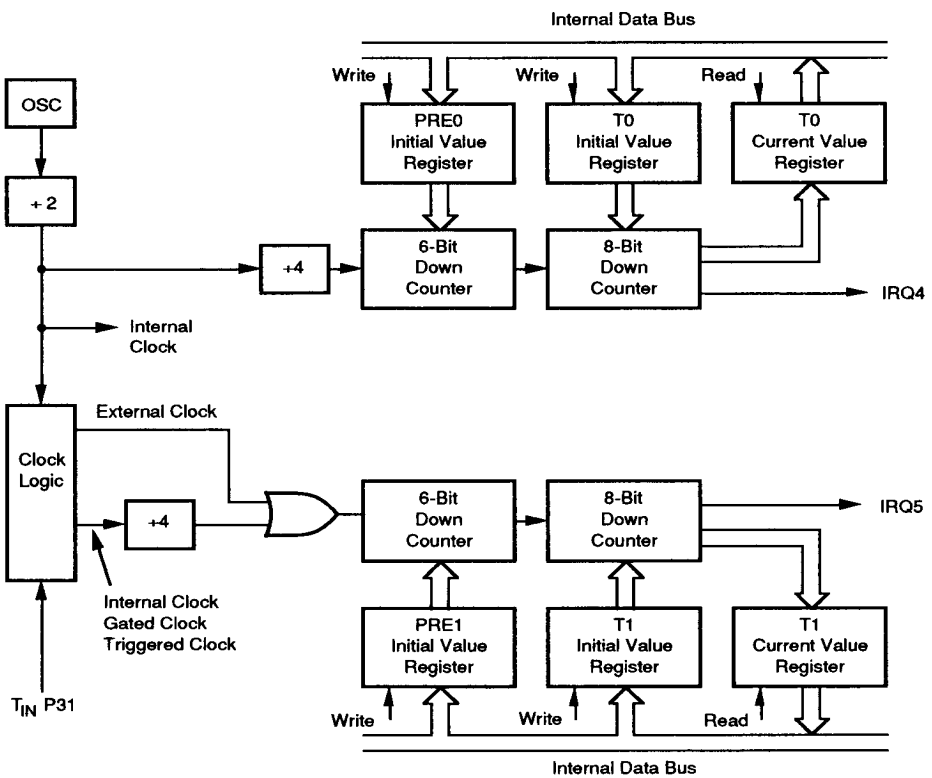


Figure 10. Counter/Timers Block Diagram

Interrupts. The Z86C08 has six interrupts from six different sources. These interrupts are maskable and prioritized (Figure 11). The six sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and the two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 3).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C08 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Table 3. Interrupt Types, Sources, and Vectors

Source	Name	Vector Location	Comments
AN2(P32)	IRQ0	0,1	External (F)Edge
REF(P33)	IRQ1	2,3	External (F)Edge
AN1(P31)	IRQ2	4,5	External (F)Edge
AN2(P32)	IRQ3	6,7	External (R)Edge
T0	IRQ4	8,9	Internal
T1	IRQ5	10,11	Internal

Notes:
F=Falling edge triggered
R=Rising edge triggered

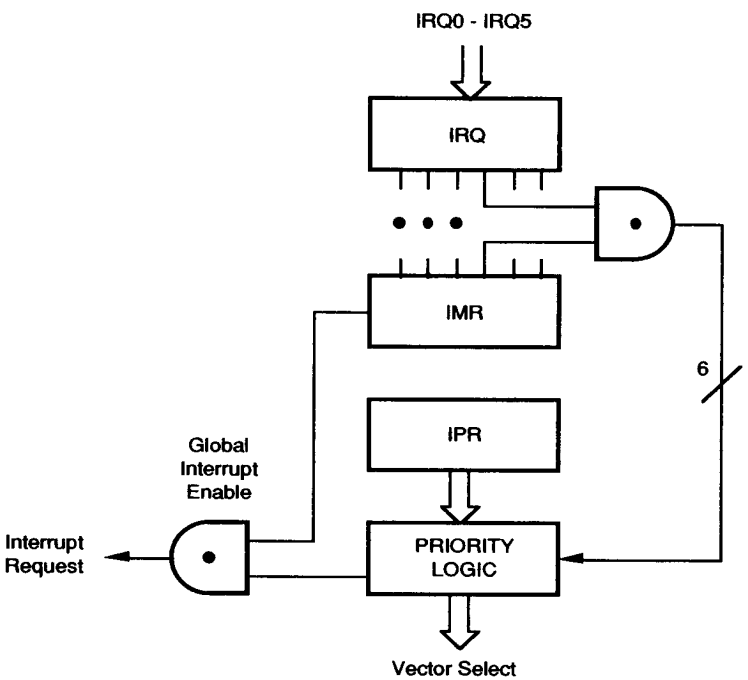


Figure 11. Interrupt Block Diagram

Clock. The Z86C08 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance is between 10 pF to 250 pF which depends on the crystal manufacturer, ceramic resonator and PCB layout) from each pin to ground (Figure 12).

HALT Mode. Turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device can be recovered by interrupts, either externally or internally generated. The program execution begins at location %000C (HEX).

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamps. The STOP Mode can be released by two methods. The first method is a RESET of the device by removing VCC. The second method is if P27 is configured as an input line when the device executes the STOP instruction. A low input condition on P27 releases the STOP Mode.

Program execution under both conditions begins at location %000C (HEX). However, when P27 is used to release the STOP Mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
OR      P2M, #%80
NOP
STOP
```

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction. i.e.:

```
FF    NOP     ; clear the pipeline
6F    STOP    ; enter STOP mode
              or
FF    NOP     ; clear the pipeline
7F    HALT    ; enter HALT mode
```

Watch Dog Timer (WDT). The Watch Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT should be refreshed once the WDT is enabled within every 15 msec; otherwise, the Z86C08 resets itself.

WDT=5F (HEX).

Opcode WDT (%5F). The first time opcode %5F is executed, the WDT is enabled, and subsequent execution clears the WDT counter. This has to be done at least every 15 msec. Otherwise, the WDT times out and generates a reset. The generated reset is the same as a power on reset of 50 msec +18 XTAL clock cycles.

Opcode WDH (%4F). When this instruction is executed it will enable the WDT during HALT. If not, the WDT will stop when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT function running during HALT Mode. A WDH instruction executed without executing WDT (%5F) has no effect.

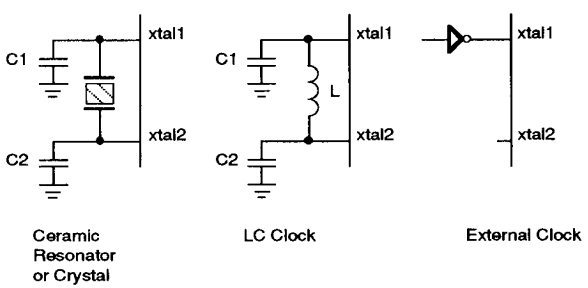


Figure 12. Oscillator Configuration

Brown-Out Protection (V_{BO}). The brown-out trip voltage (V_{BO}) is less than 3 volts and above 1.4 volts under the following conditions:

Maximum (V_{BO}) Conditions:

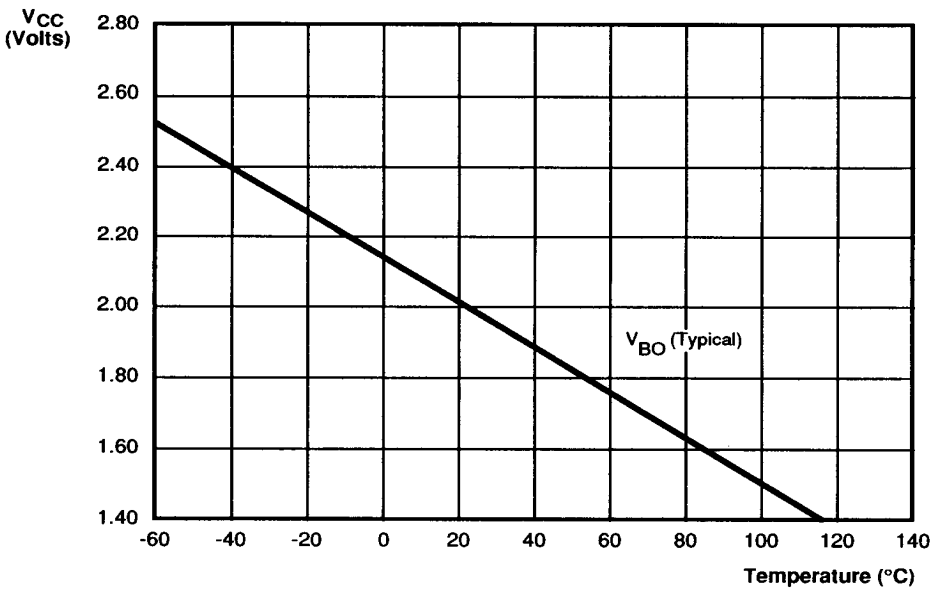
Case 1 T_A= -40°C, +105°C, Internal Clock Frequency equal or less than 1 MHz

Case 2 T_A= -40°C, +85°C, Internal Clock Frequency equal or less than 2 MHz

Note: The internal clock frequency is one half the external clock frequency.

The device will function normally at or above 3.0V under all conditions. Below 3.0V, the device functions normally until the Brown-Out Protection trip point (V_{BO}) is reached. The device is guaranteed to function normally at supply voltages above the brown-out trip point for the temperatures and operating frequencies in Case 1 and Case 2 above. The actual brown-out trip point is a function of temperature and process parameters (Figure 13).

2 MHz (Typical)					
Temp	-40°C	0°C	25°C	70°C	105°C
V_{BO}	2.55	2.4	2.1	1.7	1.6



* Power-on Reset threshold for V_{CC} and 4 MHz V_{BO} overlap

Figure 13. Typical Z86C08 V_{BO} vs. Temperature

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 14).

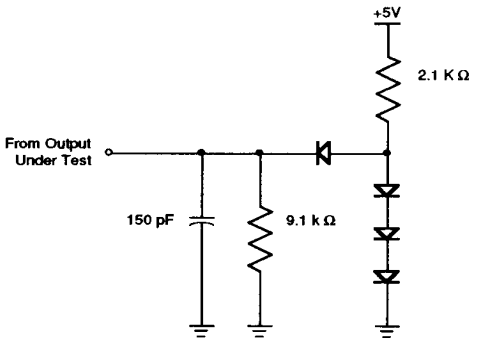


Figure 14. Test Load Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7	V
TSTG	Storage Temp	-65°	+150°	C
T_A	Oper Ambient Temp	†	†	C

Note:
*Voltages on all pins with respect to GND
† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

T_A = GND = 0V, f = 1.0 MHz, unmeasured pins to GND

Parameter	Max
Input capacitance	10 pF
Output capacitance	20 pF
I/O capacitance	25 pF

V_{CC} SPECIFICATION

Low V_{CC} 3.3V ± 0.3V
High V_{CC} 5.0V ± 0.5V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	T_A = 0°C to 70°C		T_A = -40°C to 105°C		Typical @ 25°C	Units	Conditions
			Min	Max	Min	Max			
	Max Input Voltage	3.0V		12		12		V	V_{IN} = 250 µA
		5.5V		12		12		V	V_{IN} = 250 µA
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.7	V	Driven by External Clock Generator
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.75	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	3.0V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	0.8	V	Driven by External Clock Generator
		5.5V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.8	V	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.8	V	
V_{IL}	Input Low Voltage	3.0V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	0.8	V	
		5.5V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.5	V	
V_{OH}	Output High Voltge	3.0V	V_{CC}-0.4		V_{CC}-0.4		3.0	V	I_{OH} = -2.0 mA
		5.5V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA
V_{OL1}	Output Low Voltage	3.0V		0.8		0.8	0.2	V	I_{OL} = +4.0 mA
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA
V_{OL2}	Output Low Voltage	3.0V		1.0		1.0	0.8	V	I_{OL} = +12 mA, 3 Pin Max
		5.5V		0.8		0.8	0.3	V	I_{OL} = +12 mA, 3 Pin Max
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV	
		5.5V		25		25	10	mV	
V_{BO}	V_{CC} Brown Out Voltage		1.55	2.7	1.45	2.95	2.1	V	@ 2 MHz Max, Ext. CLK Freq
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}
		5.5V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	3.0V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}
		5.5V	-1.0	1.0	-1.0	1.0		µA	V_{IN} = 0V, V_{CC}

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	T_A = 0°C to 70°C Min	Max	T_A = -40°C to 105°C Min	Max	Typical @ 25°C	Units	Conditions
I_{CC}	Supply Current	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		7.0		7.0	3.0	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 8 MHz
		5.5V		11.0		11.0	6.0	mA	All Output and I/O Pins Floating @ 8 MHz
		3.0V		10		10	3.6	mA	All Output and I/O Pins Floating @ 12 MHz
		5.5V		15		15	9.0	mA	All Output and I/O Pins Floating @ 12 MHz
I_{CC1}	Standby Current	3.0V		2.5		2.5	0.7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		5.5V		4.0		5.0	2.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 2 MHz
		3.0V		4.0		4.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz
		5.5V		5.0		5.0	3.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz
		3.0V		4.5		4.5	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
		5.5V		7.0		7.0	4.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
I_{CC2}	Standby Current	3.0V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running
		5.5V		10		20	1.0	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running
I_{ALL}	Auto Latch Low Current	3.0V		5.0		7.0	3.0	µA	$0V < V_{IN} < V_{CC}$
		5.5V		15		20	11	µA	$0V < V_{IN} < V_{CC}$
I_{ALH}	Auto Latch High Current	3.0V		-2.5		-4.0	-1.5	µA	$0V < V_{IN} < V_{CC}$
		5.5V		-7.0		-9.0	-5.0	µA	$0V < V_{IN} < V_{CC}$

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven on Crystal	3.0	5.0	mA	8 MHz
or XTAL Resonator	0.3	50	mA	8 MHz

[2] V_{SS} = 0V = GND

[3] For 2.75V operating, the device operates down to V_{BO}. The minimum operational V_{CC} is determined on the value of the voltage V_{INT} at the ambient temperature. The V_{INT} increases as the temperature decreases.

† Typical Values of V_{CC} = 3.3V and 5.0V.

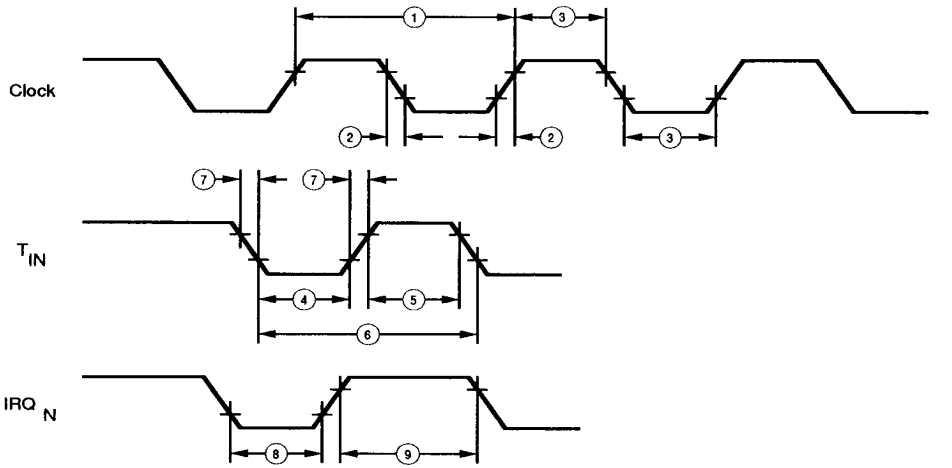


Figure 15. Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS
Timing Table

No	Symbol	Parameter	V_{cc}	T_A = 40°C TO 105°C				Units	Notes
				8 MHz		12 MHz			
				Min	Max	Min	Max		
1	TpC	Input Clock Period	3.0V	125	100,000	83	100,000	ns	[1]
			5.5V	125	100,000	83	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise	3.0V		25		15	ns	[1]
		and Fall Times	5.5V		25		15	ns	
3	TwC	Input Clock Width	3.0V	37		26			[1]
			5.5V	37		26		ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width		3TpC		3TpC			[1]
				3TpC		3TpC			[1]
6	TpTin	Timer Input Period		8TpC		8TpC			[1]
				8TpC		8TpC			[1]
7	TrTin,	Timer Input Rise			100		100	ns	[1]
	TtTin	and Fall Timer			100		100	ns	[1]
8	TwiL	Int. Request Input		100		100		ns	[1,2]
		Low Time		70		70		ns	[1,2]
9	TwiH	Int. Request Input		3TpC		3TpC			[1]
		High Time							
				3TpC		3TpC			[1,2]
10	Twdt	Watchdog Timer			25		25	ms	[1]
		Delay Time			15		15	ms	[1]

Notes:
[1] Timing Reference uses 0.9 V_{cc} for a logic 1 and 0.1 V_{cc} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).

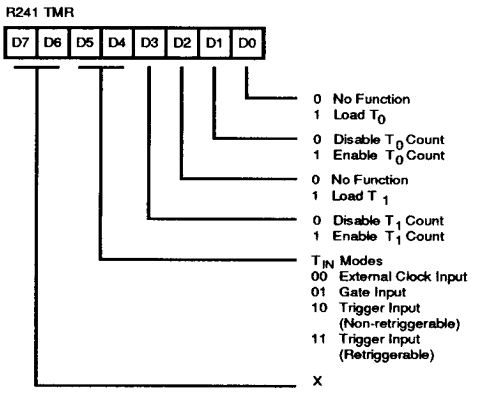


Figure 16. Timer Mode Register ($F1_H$: Read/Write)

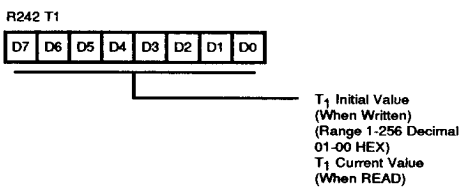


Figure 17. Counter Time 1 Register ($F2_H$: Read/Write)

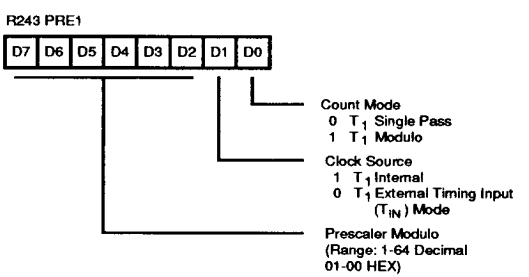


Figure 18. Prescaler 1 Register ($F3_H$: Write Only)

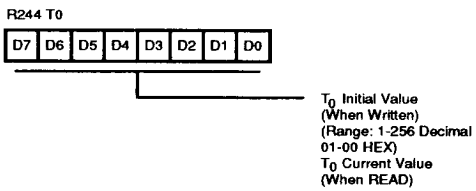


Figure 19. Counter/Timer 0 Register ($F4_H$: Read/Write)

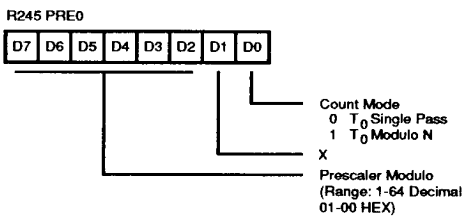


Figure 20. Prescaler 0 Register ($F5_H$: Write Only)

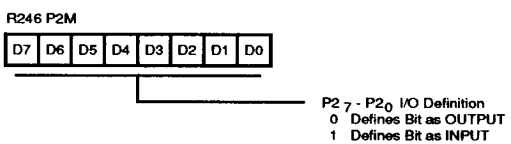


Figure 21. Port 2 Mode Register ($F6_H$: Write Only)

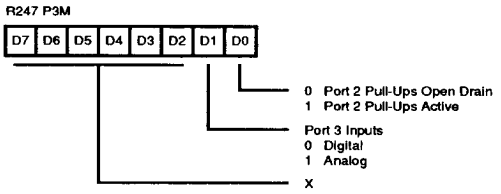


Figure 22. Port 3 Mode Register ($F7_H$: Write Only)

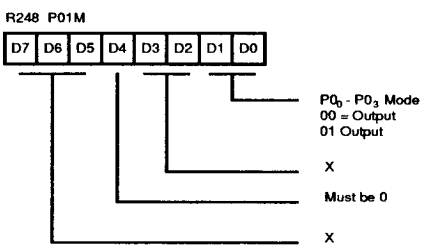


Figure 23. Port 0 and 1 Mode Register ($F8_H$: Write Only)

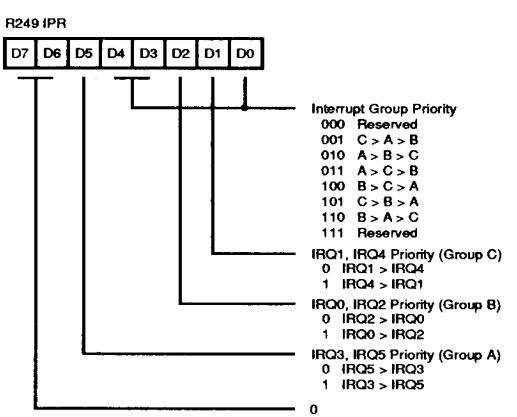


Figure 24. Interrupt Priority Register ($F9_H$: Write Only)

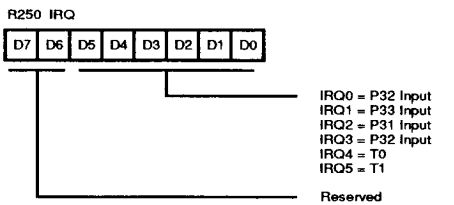


Figure 25. Interrupt Request Register (FA_H: Read/Write)

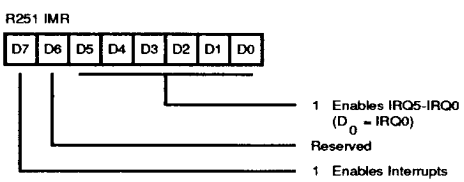


Figure 26. Interrupt Mask Register (FB_H: Read/Write)

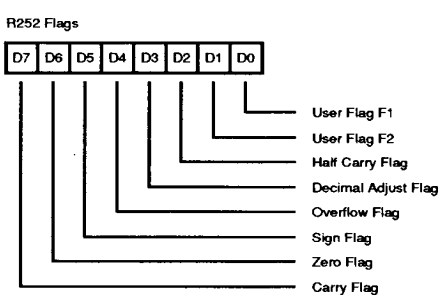


Figure 27. Flag Register (FC_H: Read/Write)

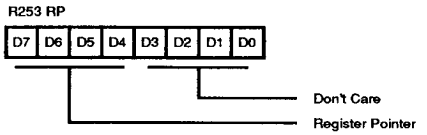


Figure 28. Register Pointer (FD_H: Read/Write)

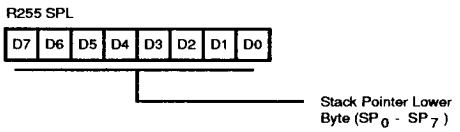


Figure 29. Stack Pointer (FF_H: Read/Write)

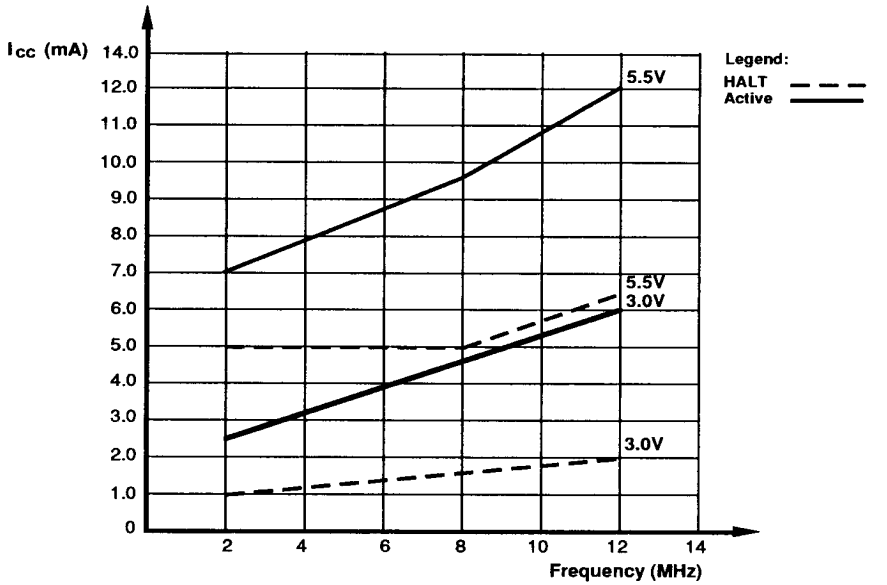


Figure 30. Maximum I_{cc} vs. Frequency

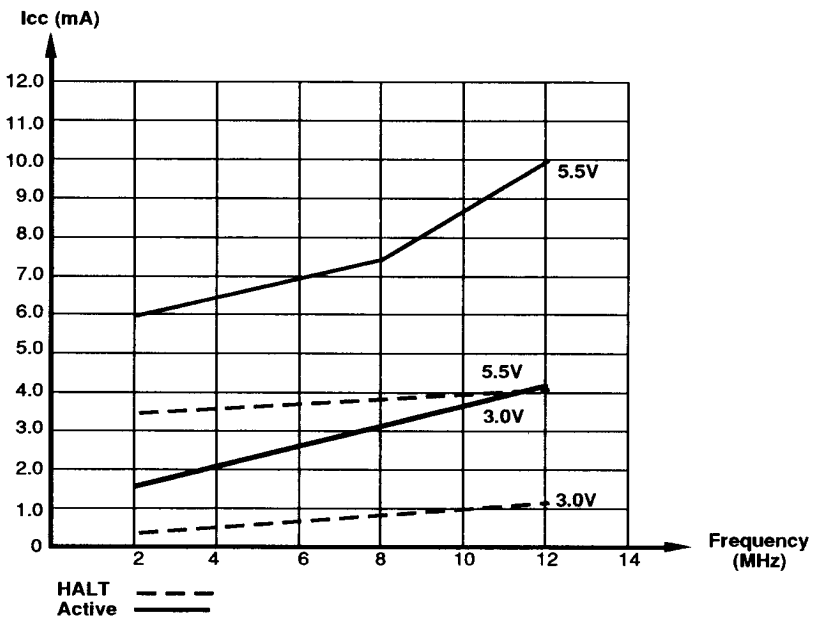


Figure 31. Typical I_{cc} vs. Frequency

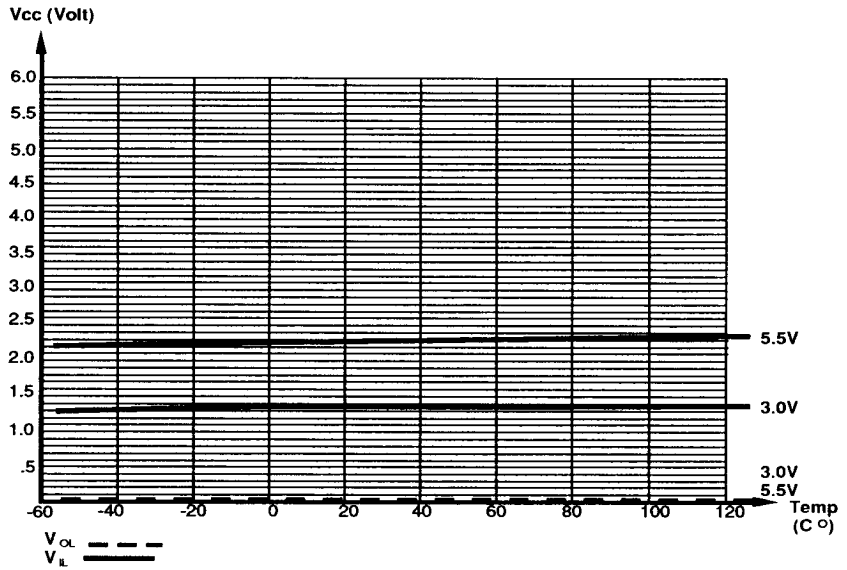


Figure 32. V_{IL}, V_{OL} vs. Temperature

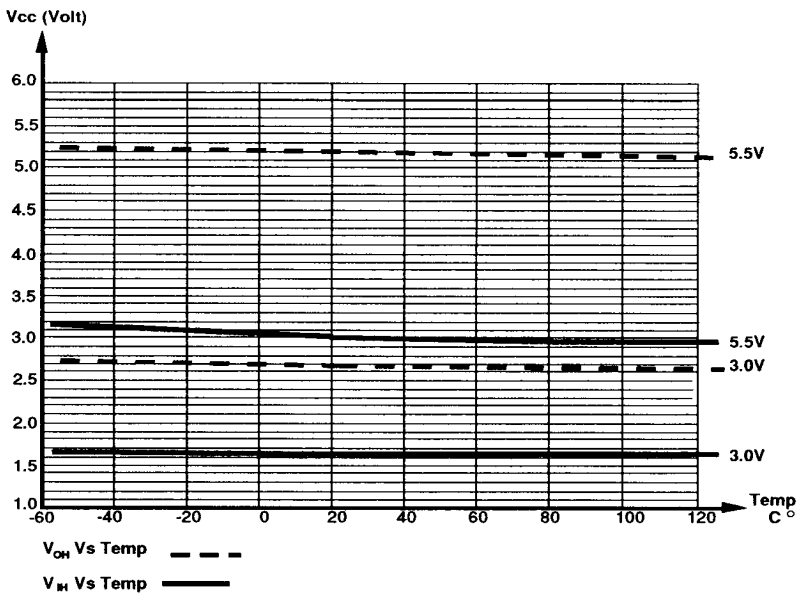


Figure 33. V_{IH}, V_{OH} vs. Temperature

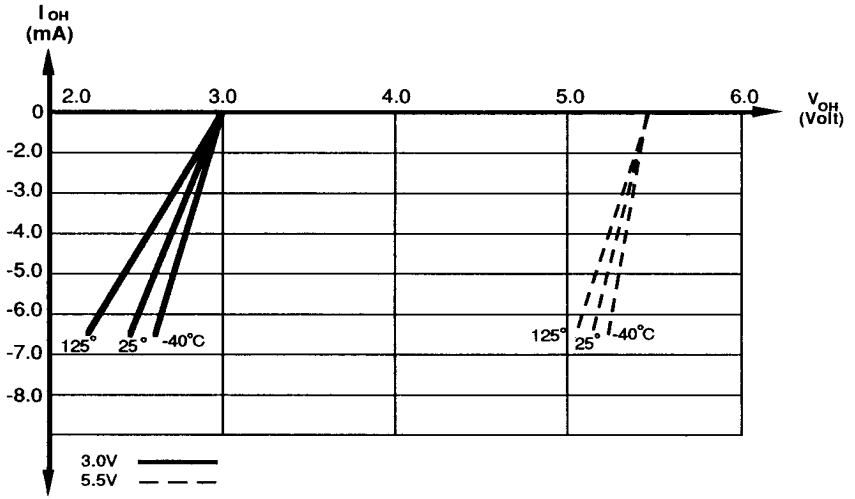


Figure 34. Typical I_{OH} vs. V_{OH}

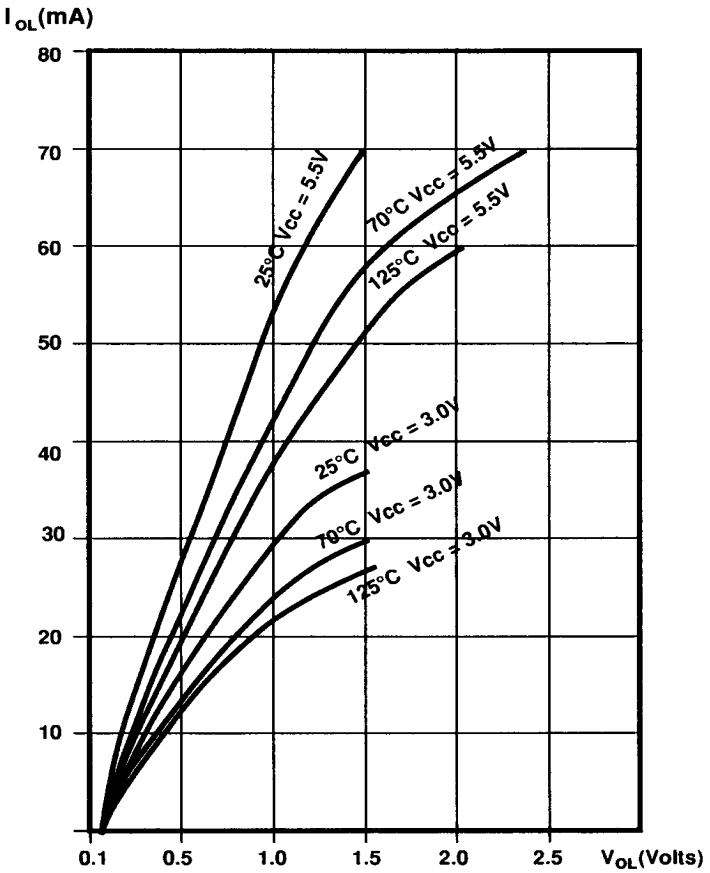


Figure 35. Typical I_{OL} vs. V_{OL}

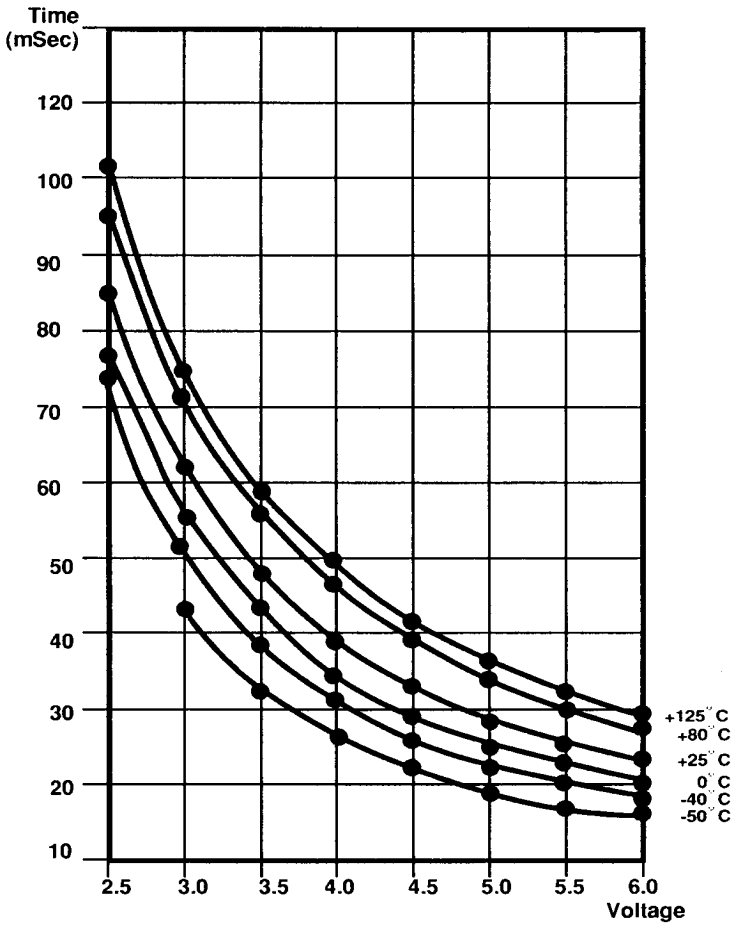


Figure 36. Typical WDT Time Out Period vs. V_{CC} Over Temperature

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Ir	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack pointer
PC	Program counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags.

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

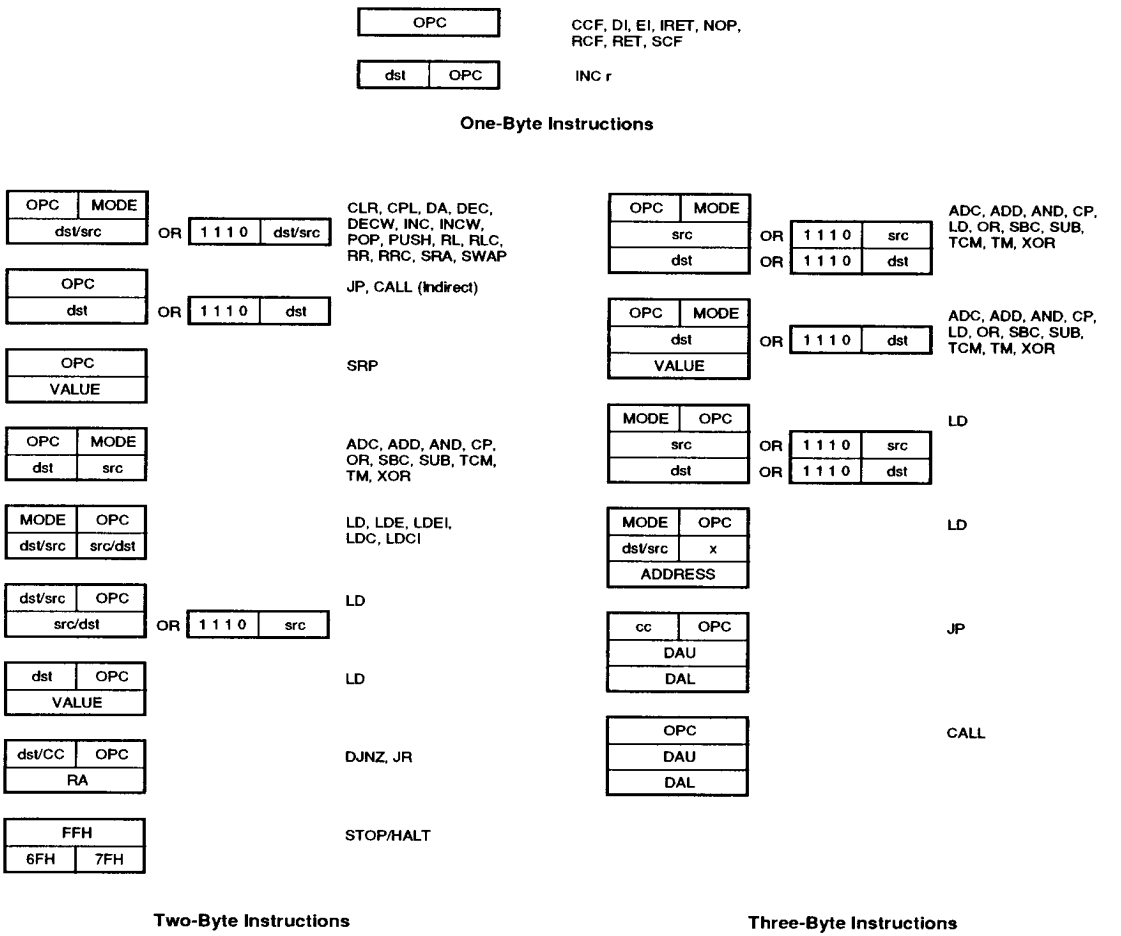
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
X	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	---	Always true	---
0111	C	Carry	C=1
1111	NC	No Carry	C=0
0110	Z	Zero	Z=1
1110	NZ	Not zero	Z=0
1101	PL	Plus	S=0
0101	MI	Minus	S=1
0100	OV	Overflow	V=1
1100	NOV	No overflow	V=0
0110	EQ	Equal	Z=1
1110	NE	Not equal	Z=0
1001	GE	Greater than or equal	(S XOR V)=0
0001	LT	Less than	(S XOR V)=1
1010	GT	Greater than	[Z OR (S XOR V)]=0
0010	LE	Less than or equal	[Z OR (S XOR V)]=1
1111	UGE	Insigned greater than or equal	C=0
0111	ULT	Unsigned less than	C=1
1011	UGT	Unsigned greater than	(C=0 AND Z=0)=1
0011	ULE	Unsigned less than or equal	(C OR Z)=1
0000	---	Never true	---

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "---". For example:

dst --- dst + src

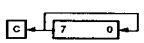
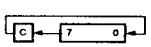
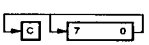
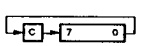
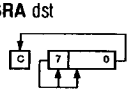
indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

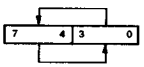
dst(7)

refers to bit 7 of the destination operand.

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r r R r r X r r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src	R IR		70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP dst RP←src	Im		31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	1	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

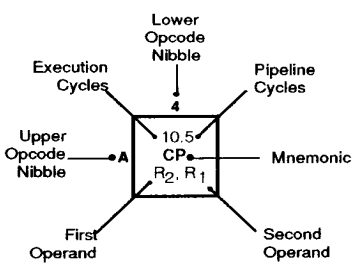
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

0PCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								4.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								5.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2				3				2				3		1	



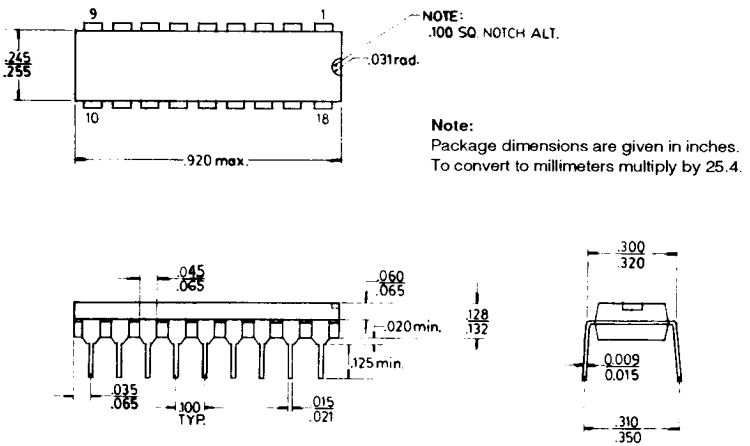
Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_1 = Dst address
R_2 or r_2 = Src address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas not defined.

* 2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION



18-Pin Dual In-Line Plastic (DIP) Package

ORDERING INFORMATION

Z86C08	
8 MHz	**12 MHz**
Z86C0808PSC	Z86C0812PSC
Z86C0808PEC	Z86C0812PEC

For fast results, contact your local Zilog sale offices for assistance in ordering the part desired.

CODES

Package
P = Plastic DIP
V = Plastic Chip Carrier
C = Ceramic DIP
L = Ceramic LCC

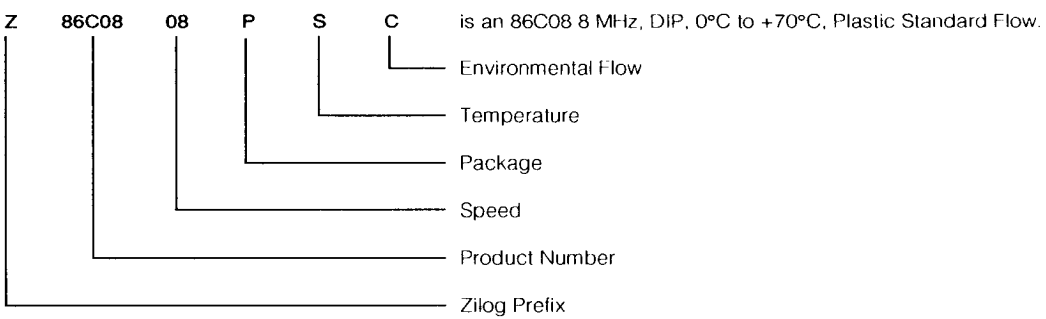
Longer Lead Time
F = Plastic Quad Flat Pack

Temperature
E = -40°C to + 105°C
S = 0°C to 70°C

Speed
08 = 8 MHz

Environmental
C = Plastic Standard

Example:



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